

## FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.8 ns at 3.3 V
- Input and Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Other Products to Consider: SN74LVC32245, SN74LVCH32245A, SN74LVCR32245A
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 32-bit (quad-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCHR32245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of this device for down translation in a mixed-voltage environment.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{OE}$  or DIR.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVCHR32245AKR	LQ245A
	LFBGA – ZKE (Pb-free)		74LVCHR32245AZKER	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



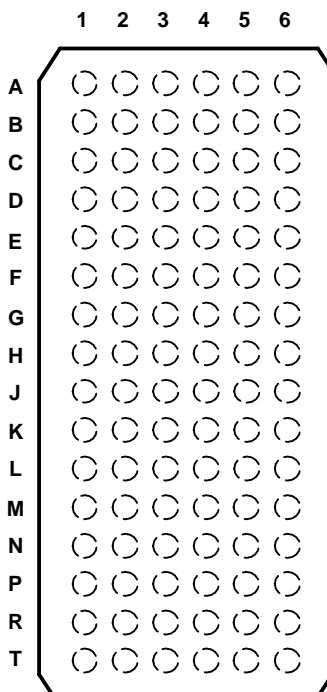
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Widebus+ is a trademark of Texas Instruments.

**SN74LVCHR32245A**  
**32-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES601–AUGUST 2004–REVISED SEPTEMBER 2005

**GKE OR ZKE PACKAGE**  
**(TOP VIEW)**



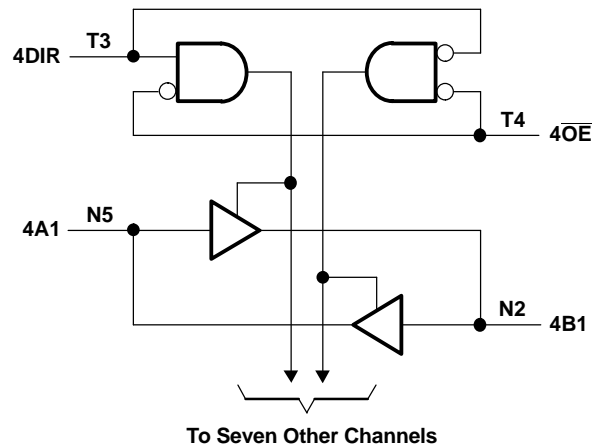
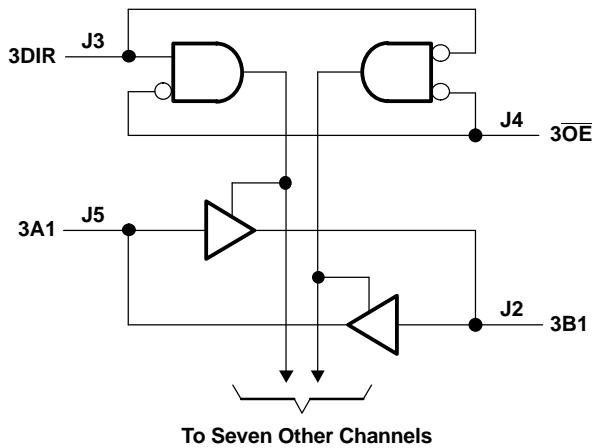
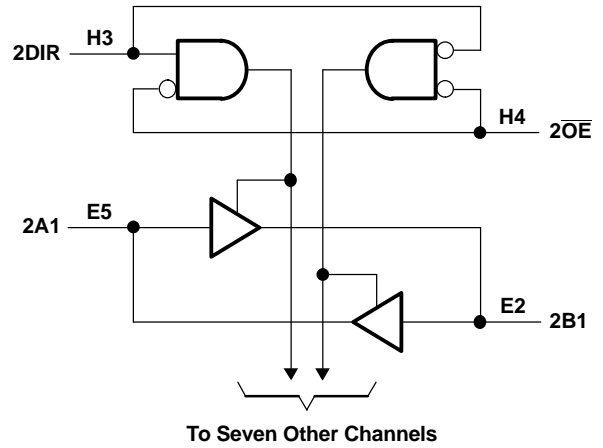
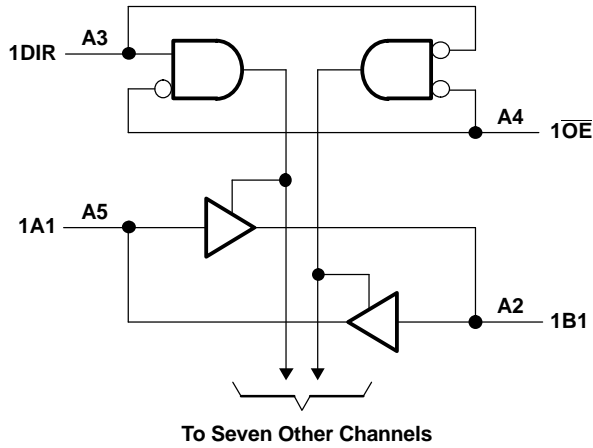
**TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6
<b>A</b>	1B2	1B1	1DIR	1 $\overline{OE}$	1A1	1A2
<b>B</b>	1B4	1B3	GND	GND	1A3	1A4
<b>C</b>	1B6	1B5	V <sub>CC</sub>	V <sub>CC</sub>	1A5	1A6
<b>D</b>	1B8	1B7	GND	GND	1A7	1A8
<b>E</b>	2B2	2B1	GND	GND	2A1	2A2
<b>F</b>	2B4	2B3	V <sub>CC</sub>	V <sub>CC</sub>	2A3	2A4
<b>G</b>	2B6	2B5	GND	GND	2A5	2A6
<b>H</b>	2B7	2B8	2DIR	2 $\overline{OE}$	2A8	2A7
<b>J</b>	3B2	3B1	3DIR	3 $\overline{OE}$	3A1	3A2
<b>K</b>	3B4	3B3	GND	GND	3A3	3A4
<b>L</b>	3B6	3B5	V <sub>CC</sub>	V <sub>CC</sub>	3A5	3A6
<b>M</b>	3B8	3B7	GND	GND	3A7	3A8
<b>N</b>	4B2	4B1	GND	GND	4A1	4A2
<b>P</b>	4B4	4B3	V <sub>CC</sub>	V <sub>CC</sub>	4A3	4A4
<b>R</b>	4B6	4B5	GND	GND	4A5	4A6
<b>T</b>	4B7	4B8	4DIR	4 $\overline{OE}$	4A8	4A7

**FUNCTION TABLE  
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74LVCHR32245A

## 32-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCES601–AUGUST 2004–REVISED SEPTEMBER 2005

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		–0.5	6.5	V
V <sub>I</sub>	Input voltage range		–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>		–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or GND			±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	GKE/ZKE package		40	°C/W
T <sub>stg</sub>	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–2	mA
		V <sub>CC</sub> = 2.3 V		–4	
		V <sub>CC</sub> = 2.7 V		–8	
		V <sub>CC</sub> = 3 V		–12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		2	mA
		V <sub>CC</sub> = 2.3 V		4	
		V <sub>CC</sub> = 2.7 V		8	
		V <sub>CC</sub> = 3 V		12	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
		I <sub>OH</sub> = -2 mA	1.65 V	1.2			
		I <sub>OH</sub> = -4 mA	2.3 V	1.7			
		I <sub>OH</sub> = -8 mA	2.7 V	2			
		I <sub>OH</sub> = -12 mA	3 V	2.4			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 2 mA	1.65 V			0.45	
		I <sub>OL</sub> = 4 mA	2.3 V			0.7	
		I <sub>OL</sub> = 8 mA	2.7 V			0.6	
		I <sub>OL</sub> = 12 mA	3 V			0.8	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>I(hold)</sub>		V <sub>I</sub> = 0.58 V	1.65 V	25			μA
		V <sub>I</sub> = 1.07 V		-25			
		V <sub>I</sub> = 0.7 V	2.3 V	45			
		V <sub>I</sub> = 1.7 V		-45			
		V <sub>I</sub> = 0.8 V	3 V	75			
		V <sub>I</sub> = 2 V		-75			
		V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>OZ</sub> <sup>(3)</sup>		V <sub>O</sub> = 0 V or (V <sub>CC</sub> to 5.5 V)	2.3 V to 3.6 V			±5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	I <sub>O</sub> = 0		40	μA
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup>				40	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			3	pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			12	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For the total leakage current in an I/O port, please consult the I<sub>I(hold)</sub> specification for the input voltage condition 0 V < V<sub>I</sub> < V<sub>CC</sub>, and the I<sub>OZ</sub> specification for the input voltage conditions V<sub>I</sub> = 0 V or V<sub>I</sub> = V<sub>CC</sub> to 5.5 V. The bus-hold current, at input voltage greater than V<sub>CC</sub>, is negligible.

(4) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1	12.5	1	9.5	1	5.7	1.5	4.8	ns
t <sub>en</sub>	$\overline{OE}$	A or B	1	15.8	1	12.2	1	7.9	1.5	6.3	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1	19.2	1	11.9	1	8.3	2.2	7.4	ns

# SN74LVCHR32245A 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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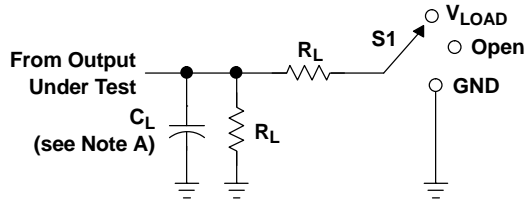
## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	(1)	(1)	39	pF
	Outputs disabled		(1)	(1)	4	

(1) This information was not available at the time of publication.

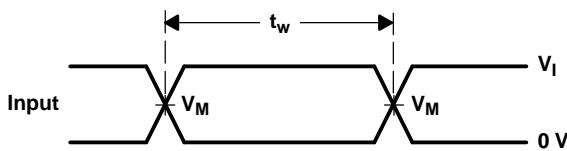
PARAMETER MEASUREMENT INFORMATION



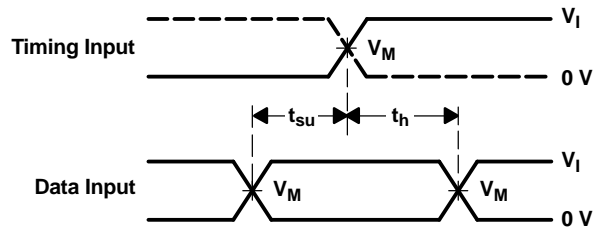
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

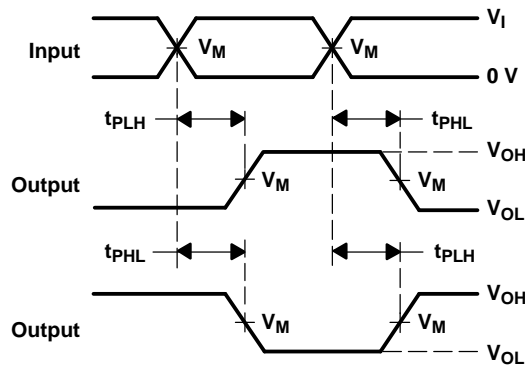
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74LVCHR32245AZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
SN74LVCHR32245AKR	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCHR32245AZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74LVCHR32245AKR	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCHR32245AZKER	LFBGA	ZKE	96	1000	346.0	346.0	41.0
SN74LVCHR32245AKR	LFBGA	GKE	96	1000	346.0	346.0	41.0

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



4204493/C 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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### Products

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
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